REMARKS

Applicants appreciate the comments of the Examiner with regards to the drawings and accordingly, a new drawing, Figure 15, has been added.

As disclosed on Page 34 of our specification, the requirement for a space that can be created between a substrate section and the cover, for example as shown in Figure 4, is not always necessary, and this space can be filled with phosphor particles as now shown in Figure 15 to support the feature of Claim 7.

Additionally, applicants appreciate the comments of the Examiner in reviewing the specification. The specification has now been corrected.

The Office Action indicated that the subject matter of Claims 5 and 9 would be allowed if rewritten in independent form. Newly drafted Claim 14 represents the allowed subject matter of Claim 5 in independent form, while newly drafted Claim 18 represents the allowed subject matter of Claim 9 in newly drafted form. Accordingly, it is believed that Claims 14-20 are allowable.

The Office Action further acknowledged receipt of our foreign priority document of Japanese Laid-Open Patent Application 2002-303508, which was filed on October 17, 2002.

To assist the Examiner, enclosed herewith is an English translation from the Japanese Patent Office of an abstract of this priority document. Applicants are in the process of translating the entire of the priority document in order to establish an effective filing date of October 17, 2002.

However, as can be seen from the Abstract, "the light reflecting layer 27 is formed in a recess 2A so as to cover the side face of the chip 26" which supports our claims.

The Office Action contended that Claims 1, 4 and 10 were rejected as obvious over *Huang* (U.S. Patent No. 6,715,901) in view of the *Zou et al* (U.S. Patent No. 6,186,649).

As can be appreciated, the *Huang* reference has an effective prior art date of March 31, 2003, which is subsequent to the effective filing date of applicants' priority document of October 17, 2002. As such, it is believed that Claims 1-4 and 10 are patentable.

The *Zou et al* reference was directed to a linear light source 102 having an concentric housing or enclosure 104 with a light emitting gap, as shown in Figure 3. A reflective layer 106 was provided on the inside of the enclosure. The Office Action specifically referred to Column 7, Lines 52-57 in order to define a primary particle size in the range of 0.1 microns to about 3.0 microns.

The present invention refers to a particle size equal or smaller than 0.5 μm. As can be appreciate, the *Zou et al* reference is not directed to an equivalent illumination system, nor does it provide the missing features purportedly relied upon in the *Huang* reference for rejecting our claims. For example, the *Zou et al* reference does not have any disclosure indicating that a light reflective layer that is made of particles of metal oxide should be provided over an insulation film thereunder, but not over the light emitting surface of the light emission chip thereunder.

The present invention provides an effect as described in Claim 1 of preventing the light reflective layer from obstructing the light from the chips by placement of the reflection surface lower than a light emission surface, so that the light reflection surface will not cover the light emission surface. Our invention further has a capacity of enhancing a heat dissipation effect by having the light reflective layer made of thermally conductive fine particles abut against the side surfaces of the chip. Thus, particles of metal oxide are provided above an insulation film and

surround the light emitting surfaces of the light emission chips to thereby further assist in thermally conducting heat away from the chip.

Claims 6 and 8 were further rejected over a combination of the *Huang, Zou et al* and the *Robertson et al* (U.S. Patent No. 6,068,383).

The *Robertson et al* reference was relied upon to teach a phosphor layer coating mounted on the back side of a transparent surface. The phosphor layer is facing light-emitting diodes which can activate the phosphorous. The light-emitting diodes are apart from, and spaced from, the phosphorous. Again, the *Robertson et al* reference does not teach the claim elements defined by the *Huang* disclosure.

Finally, Claims 11 and 12 are rejected over a combination of the *Shimizu et al* (Laid-Open Publication 2003/0189829) in view of *Robertson et al* and *Zou et al.* This reference is assigned to the assignee of the present application and discloses an LED illumination source of a card type configuration. As can be appreciated, the *Shimizu et al* reference does not disclose wavelength emission in an ultraviolet range, nor reflective layers made of particles of metal oxide. Additionally, the *Shimizu et al* reference was filed in the United States on February 26, 2003, after our priority date and the publication of the Japanese application was on April 25, 2003, as can be seen from the attached patent abstract.

Applicants respectfully submit that the *Shimizu et al* reference likewise is not prior art against the present claims. Applicants will supplement this response with the verified English translation of our priority document to assist the Examiner in this manner.

Finally, applicants have submitted an IDS disclosing the *Justel et al* (U.S. Patent No. 6,084,250) and the corresponding PCT Publication WO 98/39805. This reference discloses an LED encapsulated within a transparent coating of a matrix of polyacrylate, polystyrene, epoxy

resin or another polymer with blue, green and red emitting phosphors. This teaching is not as pertinent as the references of record and is submitted to be sure that a complete record is before the Examiner.

It is believed that the present application is now in condition for allowance upon the submission of the Certified English Translation of the priority document, and if there are any questions, the undersigned attorney would appreciate a telephone conference.

I hereby certify that this correspondence is being deposited with the United States Postal Service as First Class Mail in an envelope addressed to Commissioner for Patents, P.O. Box 1450, Alexandria, VA 22313-1450 on December 8, 2005.

By: Sharon Farnus

Signature

Dated: December 8, 2005

Very truly yours,

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IN THE DRAWINGS:

Please add the new drawing sheet of Figure 15.